AMENDMENTS TO THE CLAIMS:

Claims 1-17 are pending in the application. The claims as originally filed are presented below.

Listing of Claims:

1. (Original) A method for measuring jitter in a digital input signal, the method comprising:

producing a digital reference signal having a predetermined frequency offset from that of said digital input signal;

detecting a first occurrence of a predetermined phase relationship between said digital input signal and said digital reference signal;

detecting subsequent occurrence of said predetermined phase relationship between said digital input signal and said digital reference signal; and

determining the time difference between said first occurrence and said subsequent occurrence, to determine a measurement of jitter present in said digital input signal.

2. (Original) The method of claim 1 wherein the step of producing said digital reference signal comprises:

measuring the frequency of said digital input signal to produce a frequency measurement; and

using the frequency measurement to produce said digital reference signal having a frequency which is offset therefrom by a predetermined amount.

3. (Original) The method of claim 1 wherein the step of detecting a first occurrence of a predetermined phase relationship between said digital input signal and said digital reference signal and the step of detecting subsequent occurrence of said predetermined phase relationship between said digital input signal and said digital reference signal comprise detecting coincidence of similar edges of said digital input signal and said digital reference signal.

4. (Original) The method of claim 1 wherein the step of detecting subsequent occurrence of said predetermined phase relationship between said digital input signal and said digital reference signal comprises:

detecting over a plurality of said subsequent occurrences a maximum time difference value and a minimum time difference value; and

determining from said maximum time difference value and said minimum time difference value a total peak-to-peak jitter measurement.

5. (Original) The method of claim 4 wherein said predetermined frequency offset is varied between test cycles to facilitate detection of fixed frequency jitter based on a frequency that would beat with a fixed frequency offset.

6. (Original) The method of claim 1 further comprising pre-scaling the digital input signal to increase the resolution of jitter measurement.

7. (Original) An apparatus for measuring jitter in a digital input signal, the apparatus comprising:

a receiving arrangement for receiving a digital input signal;

a reference signal arrangement for producing a digital reference signal having a predetermined frequency offset from that of said digital input signal;

a phase detecting arrangement for detecting a first occurrence of a predetermined phase relationship between said digital input signal and said digital reference signal and subsequent occurrence of said predetermined phase relationship between said digital input signal and said digital reference signal; and

a determining arrangement for determining the time difference between said first occurrence and said subsequent occurrence, to determine a measurement of jitter present in said digital input signal.

8. (Original) The apparatus of claim 7 wherein said reference signal arrangement comprises:

a measuring arrangement for measuring the frequency of said digital input signal to produce a frequency measurement; and

a signal producing arrangement for producing from said frequency measurement said digital reference signal having a frequency which is offset therefrom by a predetermined amount.

9. (Original) The apparatus of claim 8 wherein said measuring arrangement comprises a frequency counter.

10. (Original) The apparatus of claim 8 wherein said signal producing arrangement comprises a programmable oscillator.

11. (Original) The apparatus of claim 7 wherein said phase detecting arrangement comprises an edge detecting arrangement for detecting coincidence of similar edges of said digital input signal and said digital reference signal.

12. (Original) The apparatus of claim 7 wherein said phase detecting arrangement comprises:

a minimum/maximum detecting arrangement for detecting over a plurality of said subsequent occurrences a maximum time difference value and a minimum time difference value; and

a jitter determining arrangement for determining from said maximum time difference value and said minimum time difference value a total peak-to-peak jitter measurement.

13. (Original) The apparatus of claim 12 wherein said minimum/maximum detecting arrangement comprises:

a counter arrangement driven by said reference signal;

a maximum register arrangement for holding a value in said counter arrangement when said phase detecting arrangement detects a said second occurrence;

a maximum comparator arrangement for comparing a value in said maximum register arrangement with a value in said counter arrangement when said phase detecting arrangement detects a said subsequent occurrence and if said counter arrangement value is greater than said maximum register arrangement value storing said counter arrangement value in said maximum register arrangement;

a minimum register arrangement for holding a value in said counter arrangement when said phase detecting arrangement detects a said subsequent occurrence; and

a minimum comparator arrangement for comparing a value in said minimum register arrangement with a value in said counter arrangement when said phase detecting arrangement detects a said second occurrence and if said counter arrangement value is less than said minimum register arrangement value storing said counter arrangement value in said minimum register arrangement.

14. (Original) The apparatus of claim 7 wherein the apparatus is substantially comprised in a field programmable gate array.

15. (Original) The apparatus of claim 7 wherein the apparatus is arranged to sense jitter in a telecommunications pulse code modulation (PCM) signal.

16. (Original) The apparatus of claim 7 wherein said predetermined frequency offset is varied between test cycles to facilitate detection of fixed frequency jitter based on a frequency that would beat with a fixed frequency offset.

17. (Original) The apparatus of claim 7 further comprising a pre-scaling arrangement for pre-scaling the received digital input signal to increase the resolution of jitter measurement.